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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,090	08/26/2003	Declan McDonagh	5646-113	2780

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AIC

Office Action Summary	Application No.	Applicant(s)	
	10/648,090	MCDONAGH ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-22* is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 12/20/04 has been received and entered in the case. Claims 1-22 are pending. The amendment and argument presented therein overcome the informality objection noted in the previous Office action, therefore, is withdrawn. However, the prior art rejection to claims 1-5 is not overcome, and therefore, is repeated for the reasons set forth below. This action is FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,392,462, issued to Ebuchi et al. in view of US Patent No. 6,794,912, issued to Hirata et al.

As per claim 1, Ebuchi discloses a clock generator having a clock driver (Fig. 11) therein that supports generation of a plurality of output clock signals (PH1, ..., PH10) having different frequencies (col. 13, lines 53-57, also see Fig. 25) in a range between 1 and 1/N times a frequency of an internal clock signal (shown in Fig. 11, N= 1, 2, 4 and 8) and full-period programmable skew characteristics (using select signals PHSEL[0:3] and DIVSEL[0:1] to program the phase difference. Figs. 13-23 show possible combination which can be programmed

to obtain 1ns, 2ns, ...phase difference), where N is a positive integer greater than one (shown in Fig. 11, N= 1, 2, 4 and 8).

Ebuchi does not explicitly disclose the clock generator is implemented in an integrated chip as called for in the claim.

Hirata discloses a clock generator (Fig. 1) for generating a multiphase clock signals wherein the clock generator is implemented in an integrated circuit (col. 6, lines 2-3). As notoriously well-known by an average person skilled in the art, a circuit which is integrated in a semiconductor chip is more reliable than a circuit which uses discreet components.

It would have been obvious to one skilled in the art at the time of the invention was made to implement the Ebuchi's clock generator in an integrated circuit as taught by Hirata for the motivation discussed herein above, i.e., increase the reliability.

As per claim 2, the recited internal clock generator reads on the PLL circuit 100.

As per claim 3, Ebuchi discloses a clock generator which is configured to support generation of divide-by-N clock signal having full-period programmable skew characteristics as discussed in claim 2 that is stepped in NxM time units (shown in Fig. 3, the number of inverters in the VCO is 10) and Figs. 13-23 (1ns, 2ns, 4ns and 8ns) wherein the number of time units are adjustable by selectors and switching circuits 800, 900, 610 and 710. He further explicitly disclose any combination of phase difference and frequency ratio can be implemented using his teaching (col. 16, lines 35-39).

He does not explicitly disclose the duration must be 1/M times a period of the internal clock signal where M>8 as called for in the claim.

However, as ruled by the Court that when the general condition is met, it is not inventive to vary the range of the variables. In this instant case, Ebuchi teaches several embodiments and clearly suggests that any combination of phase difference and frequency ratio can be implemented using his teaching. Varying the parameter M such that M greater than eight is not seen as an inventive feature.

It would have been obvious to one skilled in the art at the time of the invention was made to vary the M parameter to obtain the recited combination of phase difference and frequency ratio. An artisan would be motivated to modify the Ebuchi's clock generator when there is an application which requires a particular phase difference and frequency ratio of the clock signals.

As per claim 4, this claim is rejected for the same reasons and motivation discussed in claim 3, i.e., varying M parameter to any number which satisfies a product of CxF to obtain a specific combination of phase difference and frequency ratio of the output clock signals is well within the level of one skilled in the art.

As per claim 5, Ebuchi discloses a clock generator as discussed in claim 3 wherein the internal clock signal generator is a single ended VCO having 10 stages instead of a differential VCO having five stages as called for in the claim.

Hirata discloses a clock generator (Fig. 1) wherein the internal clock signal generator is a differential VCO (Fig. 3).

It would have been obvious to one skilled in the art at the time of the invention was made to replace the Ebuchi's single ended VCO having 10 stages by the Hirata's differential VCO having five stages. The motivation would be to reduce the number of stages.

Response to Arguments

3. Applicant's arguments filed on 12/20/04 have been fully considered but they are not persuasive.

Regarding the argument Ebuchi does not disclose the output clock signals having different frequencies, i.e., the output clock signals PH1-PH10 in Fig. 11 of Ebuchi have the same frequencies.

The recited limitation is met because the output clock signals having different frequencies in the Ebuchi circuit can be achieved by selecting different frequency divider circuits, i.e., divider circuits 510, 200, 400 or 500 shown in Fig. 11. Specifically, at time t1, when the frequency divider circuit 510 is selected, the output clock signals PH1-PH10 have a frequency F. At time t2, when the frequency divider circuit 200 is selected, the output clock signals PH1-PH10 have a frequency F/2. It is clear that the frequency of the output clock signals at time t1 is different from the frequency of the output clock signals at time t2. It appears that the applicant is arguing that Ebuchi does not disclose the output clock signals having different frequencies at any given time. However, nowhere in the claim having such a requirement, i.e., it merely requires the output clock signals having different frequencies.

Regarding the argument Ebuchi does not disclose the output clock signals having full period programmable skew characteristics, i.e., the skew of the output clock signals can only be adjusted to have four different skews which do not span a full period.

It is clear that the result of spanning a full period or not depends on the frequency of the output clock signal. The example in column 13, lines 20-50 clearly shows the recited limitation,

i.e., when the output clock signal has a frequency of 100MHZ, the full period is 10 nsec and the phase difference is 8 nsec.

Allowable Subject Matter

4. Claims 6-22 are allowed. These claims are allowed for the reasons noted in the previous Office action.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/17/05

Minh Nguyen
Primary Examiner
Art Unit 2816